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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
PAT00955-000, 013721-0110-999

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]	Application Number	Filed
on 03 September 2008 Signature _E. J. Pencoske_	10/002,461	01 November 2001
	First Named Inventor SLAVIN, Keith R.	
Typed or printed name Edward L. Pencoske	Art Unit 2189	Examiner ELMORE, Reba I.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
   Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
  See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
  (Form PTO/SB/96)

☑ attorney or agent of record.
  Registration number ___29,688___.

☐ attorney or agent acting under 37 CFR 1.34.

  Registration number if acting under 37 CFR 1.34 _____

E. J. Pencoske
Signature

Edward L. Pencoske
Typed or printed name

(412) 394-9531
Telephone number

03 September 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of ___1___ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/002,461

Applicant(s): SLAVIN, Keith R.

Filed: 01 November 2001

Title: Low Power, Hash-Content Addressable Memory Architecture

Art Unit: 2189

Examiner: ELMORE, Reba I.

Docket No.: PAT000955-000

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REASONS FOR REVIEW

The examiner has finally rejected claims 1-38 and 41-44, which are all of the claims in the application. Applicant hereby requests review of the final rejection prior to filing an appeal brief for the reasons set forth below.

BACKGROUND

A known problem with content addressable memories (CAMs) is that entry miss-matches are far more common than matches, so match lines are usually charged and discharged on every access. That makes CAM power consumption relatively high compared with other storage devices. The present invention includes an apparatus and a method of reducing the match line pre-charging activity for a CAM access while allowing operation at the highest possible CAM speeds. The method involves sending a comparand word to a CAM and also sending the comparand word to a set of hash circuits, one for each legal prefix length, for parallel

comparisons. For each prefix length value, that number of most significant bits is enabled from the comparand word to the corresponding hashing circuit. Each hash circuit output then goes to the address of a corresponding memory look-up which defines a region of the CAM in which, according to the known hashing behavior, a match is guaranteed to be located--if such a match exists as a CAM entry. Each memory output is decoded and combined with the others to obtain an enable bus for banks of entries within the CAM. Larger CAM banks reduce complexity in the power saving circuits, but enable more matches than the minimum required. If more (including up to all) of the CAM is enabled than is necessary, then the CAM will still work normally, but useless entry matching will occur and CAM power savings will fall.

ARGUMENT

1. The 35 U.S.C. § 112, First Paragraph rejection is improper and must be withdrawn.

In paragraph 7 of the Office action, claims 1-38 and 41-44 stand rejected under 35 U.S.C. § 112, first paragraph, for failing to comply with the written description requirement. The examiner indicates that for the delay circuit shown in figures 1 and 5, and recited in claims 4, 11, 17 [*sic* 18], 24, and 34, "nothing more than a blank box or a black box type design is depicted which fails to give any details for one of ordinary skill in the memory arts to make and use a delay circuit in conjunction with a content adjustment memory without undue experimentation" and states that the specification does not provide "sufficient technical details for essential subject matter."

First, on its face, the rejection is overly broad as the allegedly unsupported recitation does not appear in claims 1-3, 6-10, 12-17, 19-23, 25-33, and 41-44. As to those claims, the rejection should be immediately withdrawn.

Addressing the merits of the examiner's rejection, it is respectfully submitted that the time required to enable or precharge a content addressable memory would be readily apparent to a person of ordinary skill in the art based on the specifications for the memory such that experimentation would be unnecessary. Knowing the time needed to precharge the memory based on the memory's specifications, those of ordinary skill in the memory art would be easily capable of designing a circuit to provide the necessary delay. For example, when command signals are received in a memory in advance of address signals, it is notoriously well known in the art that the execution of the command signals must be coordinated with the decoding of the address signals. For the examiner to state that a person of ordinary skill in the memory art would

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not know how to construct a delay circuit based on known precharging times is completely without foundation in the record. Applicant respectfully notes that specifications are written for persons of ordinary skill in the art and preferably omit details that are well known to such persons. *Genetech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361 (Fed. Cir. 1997).

The examiner's citation of *Automotive Technologies International, Inc. v. BMS of North America, Inc.*, 501 F.3d 1274 (Fed. Cir. 2007) does not support the examiner's position for at least the following reasons:

- That case involved a situation where a <u>mechanical</u> side impact sensor was disclosed in detail but the claims recited an <u>electronic</u> side impact sensor. There is no dichotomy in the instant application between what is disclosed and what is claimed.

- The court stated that "the novel aspect of this invention is using a velocity-type sensor for side impact sensing." <u>Thus, the specification in the case cited by the examiner was silent precisely at the "point of novelty."</u> The instant applicant has neither in the specification nor during prosecution argued that the delay circuit is novel or that the delay circuit is the "point of novelty" or even "essential subject matter."

- The specification in the case cited by the examiner stated that side impact sensing is a new field. <u>There is no corresponding statement in this case that the construction of delay circuits is a new field</u>.

- The court had testimony that indicated that a "great deal of experimentation" would have been necessary to make an electronic side impact sensor after reading the specification in the case cited by the examiner. <u>No evidence that a great deal of experimentation would be required to construct a delay circuit is in the record in the instant application.</u>

Recitation of "a delay circuit" is analogous to the recitation of "a motor," "an amplifier," or any of hundreds of well-known components. Where such components are not the focus of the invention, nothing more than a generic recitation is needed. The rejection under 35 U.S.C. § 112, first paragraph, of claims 1-38 and 41-44 based on an alleged failure to provide a written description of the delay circuit should be withdrawn.

2. The Claim Rejections Under 35 U.S.C. § 102(e) are not proper and should be withdrawn.

Beginning at paragraph 10 of the Office action, claims 41-44 are rejected under 35 U.S.C. § 102(e) as being anticipated by Cheriton (US 7,002,965).

Applicant respectfully points out that the cited portions of Cheriton do not disclose a method of _initializing_ the TCAM/CAM classifier and disclose only methods for _classifying and routing_ data packets. Therefore, at most, the cited portions of Cheriton disclose only the inherent method of initializing the TCAM/CAM classifier to operate to classify and route data packets. The TCAM/CAM classifier disclosed by the cited portions of Cheriton does not have a CAM divided into a plurality of banks and an output memory device responsive to a CAM divided into a plurality of banks. Therefore, the inherent method for initializing the TCAM/CAM classifier will be different from the claimed method because the methods for initializing different hardware are inherently different. To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. See MPEP 2112. Accordingly, it is believed that independent claim 41 as well as dependent claims 42-44 are in condition for allowance.

3. The Claim Rejections Under 35 U.S.C. § 103(a) are improper and should be withdrawn.

Beginning at paragraph 15 of the Office action, claims 1-38 are rejected under 35 U.S.C. § 102(e) as being obvious over Hariguchi et al. (US 6,665,297) in view of Cheriton. The Office correctly points out on page 7 of the Office action that Hariguchi, "does not specifically teach using hash signals to enable portions of a CAM." The Office relies on Cheriton to supply the missing teachings.

The portions of Cheriton cited by the Office disclose a TCAM/CAM classifier for classifying and routing data packets. The TCAM/CAM classifier has a CAM (See figure 3, Ref. No. 305) that stores a hash directory of network IP addresses. The CAM performs a comparison between a received hash index based on a flow label of a data packet and the _entire hash directory_ of network IP addresses. The CAM selects the network IP address for routing the data packet based on a match during the comparison of the received hash index and the _entire hash directory_ of network IP addresses (See col. 3, lines 18-21 and col. 6, lines 47-49). The cited

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portions of Cheriton do not teach using hashing signals to enable portions of a CAM and instead teach the entire CAM being responsive to hash signals. Therefore, modifying the router disclosed by Harguchi to contain a CAM responsive to hash signals instead of destination addresses does not teach or suggest enabling portions of the CAM in response to the hash signals, but rather the modification teaches a CAM being responsive to a different type of input signal. Combining the teachings of the two references does not produce the benefit of reduced power saving achieved by the claimed invention. Accordingly, it is believed that claims 1-38 are in condition for allowance.

A Notice of Allowance for pending claims 1-38 and 41-44 is respectfully requested.

Respectfully submitted,

Edward L. Pencoske
Reg. No. 29,688
Jones Day
One Mellon Center
500 Grant Street, Suite 3100
Pittsburgh, PA, USA, 15219
Direct No.: (412) 394-9531
Facsimile No.: (412) 394-7959
Attorney for Applicant